UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/714,956	11/20/2000	Petter Johnsen	3842-5	7390

7590 12/01/2003

NIXON & VANDERHYE P.C.
1100 North Glebe Rd., 8th Floor
Arlington, VA 22201-4714

EXAMINER	
NGUYEN, ANH T	
ART UNIT	PAPER NUMBER
2127	4

DATE MAILED: 12/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/714,956	JOHNSEN ET AL.	
	Examiner	Art Unit	
	Anh T Nguyen	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is responsive to application 09/714,956, filed 11/20/2000.

2. Claims 1-13 are presented for examination.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

4. The disclosure is objected to because of the following informalities:

   Page 3, line 7, "form" should recite --from--.

   Appropriate correction is required.

Claim Objections

5. Claim 1 is objected to because of the following informalities:

   Line5, "ore" should recite --or--.

   Appropriate correction is required.

6. Claims 2-13 objected to because of the following informalities:

   "characterised" should recite --characterized--.

   Appropriate correction is required.

7. Claims 9 and 10 are objected to because of the following informalities:

   "temporary" should recite --temporarily--.

   Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-13 are narrative in format and excessively use alternative expressions "or" and "and/or" rendering the intended metes and bounds at best confusing. Additionally, Claim 9 recites the limitation "PID of the receiving SP" in claim 1. There is insufficient antecedent basis for this limitation in the claim. The claims are treated with respect to prior art below as best understood by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harish Patil and Charles Fischer, "Efficient Run-Time Monitoring Using Shadow Processing", Presented at

AADEBUG'95 (Automated and Algorithmic Debugging), University of Wisconsin--Madison, pp.1-14.(hereinafter Patil) in view of Johnson et al. (USPN 4,530,051) (hereinafter Johnson).

Regarding Claim 1:

Patil discloses a shadow processing system, characterized in a virtual link handler (VLH) comprising at least one shadow process (SP) for each actual process communicating with at least one actual process and a driver communicating with at least one SP to perform tasks in multiprocessor workstations (Patil, FIGURE 1 and FIGURE 4, page 2 and 8).

However, Patil does not particularly disclose an arrangement for inter processor (CPU) or inter computer process signal communication in a system comprising two or more CPUs or computers, wherein CPUs or computers include independent operating systems (OS), inter CPU or computer communications drivers and driver associated interconnections between the CPUs or computers.

Johnson discloses the arrangement for inter processor (CPU) or inter computer process signal communication in a system comprising two or more CPUs or computers, wherein CPUs or computers include independent operating systems (OS), inter CPU or computer communications drivers and driver associated interconnections between the CPUs or computers (Johnson, Fig. 1, col.4, lines 1-13, "The multiprocessor system comprises a number of essentially identical interface module processors of which three are shown (100, 101, 102), and a central processor 120. Additionally, the switch modules, e.g., 111, of the interface module processor are interconnected by a communications medium"). Johnson also discloses the use of "The data

link controller attached to a data link (i.e. VLH – Virtual Link Handler) is provided to convey messages between processors" (Johnson, Fig. 1, col.4, lines 26-28).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the shadow processing system of Patil such that it utilizes the arrangement for inter processor (CPU) or inter computer process signal communication in a system comprising two or more CPUs or computers, wherein CPUs or computers include independent operating systems (OS), inter CPU or computer communications drivers and driver associated interconnections between the CPUs or computers disclosed by Johnson.

One of ordinary skill in the art would be motivated to do so because it simplifies the task of invoking or calling for the execution of the different procedures required to execute a process because the actual processes are statically associated with the home processor while the shadow processes which are identical to that of the actual processes will reside on a remote processor. This improvement over the prior art would eliminate the need for intra process messages to be sent among different processors and allow the execution of a process by two or more processors without substantial increase in system overhead.

Regarding Claim 2:

Patil discloses that a shadow process associated with a CPU or computer of the system is identified by a process identifier (PID) identical to the PID of the actual process associated with a another CPU or computer of the system (Patil, page 2, paragraph 1, " the shadow program to be an exact copy of shadow program").

Regarding Claim 3:

Patil discloses that a shadow process identifier (SPID) is assigned to each process (Patil, page 5, paragraph 2, " Each heap object in the main process has a slot in the shadow heap containing an *identifying* integer that is a *key* for the object").

Regarding Claim 4:

Patil discloses that the SPID itself is a unique process identifier throughout the system (Patil, page 5, paragraph 2, " This slot store the (essentially) *unique key* value").

Regarding Claim 5:

Patil discloses that the SPID in conjunction with the processor or computer address is a unique process identifier throughout the system (Patil, page 5, paragraph 2, "stores the (essentially) *unique key* value. Key values are assigned using a global counter").

Regarding Claim 6:

Patil discloses that actual processes are statically associated with or residents of particular CPUs or computer of the system (Patil, see Fig.1& Fig.4, page 1, paragraph 3, "The basic idea is to partition an executable program into two run-time processes as shown in Figure 1. One is the main process, executing as usual. The other is a shadow process. The two processes may communicate and synchronize during execution.").

Regarding Claim 7:

Patil discloses that the VLH maintains a reference list of the associations of the actual processes with the respective CPUs or computer of the system (Patil, see Fig.2, page 3, section 2, "Each pointer in the main process has a guard G_p in the shadow. The guard for a pointer stores spatial and temporal attributes for the pointer's *referent*.").

Regarding Claim 8:

Patil discloses that address tables located at each communicating CPU or computer of the system are developed from the reference list (Patil, see Fig.2, page 4, paragraph 2, "Valid pointers contain *addresses* of data objects (including pointers) or functions.").

Regarding Claim 9:

Patil discloses that a signal communicated from one process on one CPU or computer to another process on another CPU or computer is temporarily modified to include at least the PID of the receiving SP (Patil, see Fig.1& Fig.4, page 1, paragraph 3, "The basic idea is to partition an executable program into two run-time processes as shown in Figure 1. One is the main process, executing as usual. The other is a shadow process. The two processes may *communicate* and synchronize during execution.").

Regarding Claim 10:

Patil discloses that a signal communicated from one process on one CPU or computer to another process on another CPU or computer is temporarily modified to include at least the PID of the sending SP (Patil, see Fig.1& Fig.4, page 1, paragraph 3, "The basic idea is to partition an

executable program into two run-time processes as shown in Figure 1. One is the main process, executing as usual. The other is a shadow process. The two processes may *communicate* and synchronize during execution.").

Regarding Claim 11:

Patil discloses that the DA of a CPU or computer is provided with an interface to SP and/or OS associated with the same CPU or computer a signal communicated from one process on one CPU or computer to another process on another CPU or computer is temporarily modified to include at least the PID of the receiving SP (Patil, see Fig.1& Fig.4, "driver.c").

Regarding Claim 12:

Patil discloses that the DA of a CPU or computer is provided with an interface to the drivers for CPU or computer interconnections associated with the same CPU or computer (Patil, see Fig.1& Fig.4, "driver.c").

Regarding Claim 13:

Patil discloses a shadow processing method comprising the steps of:

- transferring on a CPU or computer a signal intended for another process from an originating process to a shadow process representing the other process (Patil, FIGURE 1 and FIGURE 4, page 2 and 8),
- amending parameters of the signal by means of the shadow process and a table including the system address of the other process (Patil, FIGURE 1 and FIGURE 4, page 2 and 8),

- transferring the amended signal to the other CPU or computer by means of driver adapters, the drivers and the driver associated interconnections (Patil, FIGURE 1 and FIGURE 4, page 2 and 8),
- receiving the amended signal on the other CPU or computer by a shadow process representing the originating process of the signal (Patil, FIGURE 1 and FIGURE 4, page 2 and 8),
- amending the received signal by the receiving shadow process by means of parameters carried by the received signal (Patil, FIGURE 1 and FIGURE 4, page 2 and 8), and
- transferring the amended received signal to the other process for which the signal was intended (Patil, FIGURE 1 and FIGURE 4, page 2 and 8).

However, Patil does not particularly disclose an arrangement for inter processor (CPU) or inter computer process signal communication in a system comprising two or more CPUs or computers, wherein CPUs or computers include independent operating systems (OS), inter CPU or computer communications drivers and driver associated interconnections between the CPUs or computers.

Johnson discloses a system comprising two or more CPUs or computers, wherein CPUs or computers include independent operating systems (OS), inter CPU or computer communications drivers and driver associated interconnections between the CPUs or computers (Johnson, Fig. 1, col.4, lines 1-13, "The multiprocessor system comprises a number of essentially identical interface module processors of which three are shown (100, 101, 102), and a central processor 120. Additionally, the switch modules, e.g., 111, of the interface module processor are interconnected by a communications medium"). Johnson also discloses the use of "The data

link controller attached to a data link (i.e. VLH – Virtual Link Handler) is provided to convey messages between processors" (Johnson, Fig. 1, col.4, lines 26-28).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the shadow processing system of Patil such that it utilizes the system comprising two or more CPUs or computers, wherein CPUs or computers include independent operating systems (OS), inter CPU or computer communications drivers and driver associated interconnections between the CPUs or computers disclosed by Johnson.

One of ordinary skill in the art would be motivated to do so because it simplifies the task of invoking or calling for the execution of the different procedures required to execute a process because the actual processes are statically associated with the home processor while the shadow processes which are identical to that of the actual processes will reside on a remote processor. This improvement over the prior art would eliminate the need for intra process messages to be sent among different processors and allow the execution of a process by two or more processors without substantial increase in system overhead.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form PTO-892.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh T Nguyen whose telephone number is (703) 305-8649. The examiner can normally be reached on Monday-Friday from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Grant, can be reached on (703) 308-1108. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-5484.

Anh T.Nguyen
Art Unit 2127
November 24, 2003

WILLIAM GRANT
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
11/25/03